

# UNITED STATES DEPARTMENT OF COMMERCE

## **Patent and Trademark Office**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		A	TTORNEY DOCKET NO.
09/208,325	12/09/9	8 SHIELDS		J	120998
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Anthem AZ	85086			2813	5
				DATE MAILED:	<b>ر</b> 09/14/00

Please find below and/or attached an Office communication concerning this application or proceeding.

**Commissioner of Patents and Trademarks** 





Office Action Summary

Application No. 09/208,325

Applicant(s)

Shields et al.

Examiner

Thanh Nguyen

Group Art Unit 2813



X Responsive to communication(s) filed on Jul 12, 2000	·				
X This action is FINAL.					
☐ Since this application is in condition for allowance except for for in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.					
A shortened statutory period for response to this action is set to exis longer, from the mailing date of this communication. Failure to reapplication to become abandoned. (35 U.S.C. § 133). Extensions 37 CFR 1.136(a).	espond within the period for response will cause the				
Disposition of Claims					
	is/are pending in the application.				
Of the above, claim(s) none	is/are withdrawn from consideration.				
Claim(s)	is/are allowed.				
	is/are rejected.				
☐ Claim(s)	is/are objected to.				
☐ Claims are subject to restriction or election requirement.					
Application Papers  See the attached Notice of Draftsperson's Patent Drawing Re The drawing(s) filed on is/are objected to The proposed drawing correction, filed on The specification is objected to by the Examiner.	to by the Examiner.				
☐ The oath or declaration is objected to by the Examiner.					
Priority under 35 U.S.C. § 119  Acknowledgement is made of a claim for foreign priority und All Some* None of the CERTIFIED copies of the received. received in Application No. (Series Code/Serial Number received in this national stage application from the Interaction of the CERTIFIED copies of the Priority under the Interaction of the	e priority documents have been  r) ernational Bureau (PCT Rule 17.2(a)).				
Attachment(s)					
<ul> <li>☒ Notice of References Cited, PTO-892</li> <li>☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)</li> <li>☐ Interview Summary, PTO-413</li> <li>☐ Notice of Draftsperson's Patent Drawing Review, PTO-948</li> <li>☐ Notice of Informal Patent Application, PTO-152</li> </ul>	·				
SEE OFFICE ACTION ON THE	FOLLOWING PAGES				



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#### **DETAILED ACTION**

## Response to Arguments

Applicant's arguments with respect to claims 1, 3-5 have been considered but are moot in view of the new ground(s) of rejection.

#### Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim 1 are rejected under 35 U.S.C. 102(e) as being anticipated by Xing et al. (U.S. Patent No. 5,880,026).

Referring to figures 1-3D, Xing et al teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer of metal (210, 230, 240, 250) on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on the final layer of metal; forming a first layer of photoresist (200) on the layer of TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and the final layer of metal exposing portion of



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interlayer dielectric, wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing remaing portions of the layer of TiN (see figure 2C); and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280).

### Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xing et al. (U.S. Patent No. 5,880,026) in view of the Admitted Prior Art.

Referring to figures 1-3D, Xing et al teaches a method of manufacturing a semiconductor device, wherein the method comprises: forming a final layer of metal (210, 230, 240, 250) on a layer of interlayer dielectric (270) in the semiconductor device; forming a layer of TiN (205) on



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the final layer of metal; forming a first layer of photoresist (200) on the layer of TiN; patterning and developing the first layer of photoresist exposing portions of the layer of TiN (see figure 2A and related text); etching holes in the layer of TiN and the final layer of metal exposing poriton of interlayer dielectric, wherein metal structures are formed; removing the first layer of photoresist (see figure 2B and related text); removing remaing portions of the layer of TiN (see figure 2C); and forming a blanket layer of interlayer dielectric on the surface of the semiconductor device (280).

However, the reference does not teach depositing a second photoresist layer, patterning and etching the layer of photoresist and blanket layer to exposed the metal layer, etching the photoresist layer and TiN layer by suing fluorine containing gas chemistry at an elevated temperature.

Referring to figures 1a-1I, the Admitted Prior Art teaches a method of manufacturing a semiconductor device comprises: forming a final metal layer (104) over the interlayer dielectric (102), forming a TiN layer (106) over the metal layer, forming a layer of photoresist (108) over the TiN layer, patterning and developing the first layer of photoresist exposing portions of the TiN layer, etching in the layer of TiN and the final layer of metal exposing portions of the interlay dielectric layer, removing the first layer of photoresist and the layer of TiN, depositing a blanket layer (114), forming a second photoresist layer (116) on the blanket layer of interlayer dielectric; patterning and developing the second layer of the photoresist layer exposing portions of blanket layer of interlayer dielectric overlying metal structures; and etching the exposed portion of the

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blanket layer of interlayer dielectric down to the metal structures, removing the second layer of the photoresist (see figures 1a-1I of the Admitted Prior art and related text).

Therefore, it would have been obvious to one of ordinary skill in the requisiste art at the time the invention was made would form a second photoresist layer, patterning and etching the layer of photoresist and blanket layer to exposed the metal layer as taught by the Admitted Prior art in process of Xing et al because the technique is known in manufacturing a semiconductor device.

The examiner takes Official Notice that the embodiment described in claim 5 would have been obvious to skilled worker in the art at the time the invention was made because determining the optimum material for etching the layer only involved routine skill in the art (see MPEP 2144.03).

#### Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the

statutory period for response expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Thanh Nguyen whose telephone number is (703) 308-9439. The examiner

can normally be reached on Monday-Thursday from 7:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Charles Bowers, can be reached on (703) 308-2417. The fax phone number for this Group is

(703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Thanh Nguyen

September 12, 2000

Charles Bowers

Supervisory Patent Examiner Technology Center 2800

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